A 1-W High-Efficiency Q-Band MMIC Power Amplifier

James C. L. Chi, J. A. Lester, Y. Hwang, P. D. Chow, and M. Y. Huang

***Abstract*—Recent development on MMIC power amplifier has pushed the power-added efficiency (PAE) of 1-W amplifier to 29.4%. The power amplifier, using 0.15-μm InGaAs T-gate PHEMT devices, can deliver 1.2 W with 25% efficiency at 40 GHz when the drain is biased at 5 V. When the drain voltage drops to 4 V the output power is 1 W with 9-db associated gain and 29.4% PAE. The measured linear gain is averaged to be 12.5 db from 38–44 GHz.**

I. Introduction

THE adoption of monolithic components in modern microwave and millimeter systems has become a overwhelming trend because systems require lighter weight, higher integration, and better performance at lower cost. So far, many MMIC components have been developed to perform various functionalities in almost every microwave and millimeter system. High-efficiency MMIC power amplifier is one of the key components to achieve the advanced next-generation systems. Rapid progress on high-efficiency power HEMT technology has been documented in several design applications in Ka and Q bands. Among them, Lam *et al.* developed a InP-based HEMT power amplifier that can deliver 250 mW output power with 33% efficiency at 44 GHz [1] . Meanwhile, Chen *et al.* demonstrated a MMIC power amplifier with 1-W output power and 15% efficiency at 44.5 GHz [2]. In this paper, we present the work on developing a high-power and high-efficiency MMIC power amplifier that is illustrated in Fig. 1. The output power peaked at 40 GHz is measured to be 1.2 W, nearly 460 mW/mm power density, with 25% efficiency when the drain stage is biased at 5 V. If the drain bias voltage is reduced to 4 V, 1 W output power is measured with 9-dB associated gain and 29.4% power-added efficiency.

II. Design Approach

The devices used in this work are pseudomorphic InGaAs T-gate HEMT's with 0.15-μm gate length whose characteristics are detailed in [3]. The devices are passivated with a thin layer (about 500 A) of silicon nitride. A large signal model was developed for the device with 200-μm gate width. The device modeling was based on the method of fitting measured IV curve that was described in [4]. A linear model was also developed based on the on-wafer probe measurement at multiple bias conditions. The small signal S parameters generated from the nonlinear model are in good agreement with linear model results up to 50 GHz. The device models used in harmonic balance simulation for actual devices are then scaled based on these 200-μm models. The MMIC power amplifier is a two-stage design with a schematic shown in Fig. 2. In the first stage, four 240-μm devices are used to drive the power stage, which includes eight 320-μm devices. The optimum load condition has been determined by load-pull large signal simulation. Microstrip transmission lines are designed to matching the device impedance and also combining the devices to the real 50-ohm load. Both gate and drain stages can be biased from either side of MMIC chip.

The MMIC power amplifier is stabilized through two ways: the RC biasing circuit using thin film resistor employed in gate bias line and resistive loading presented at the input to absorb excessive gain. The thin film resistors are also placed between devices to prevent the odd-mode oscillation which frequently occurs when combing many power devices. The overall chip size is 5 by 2.6 mm.

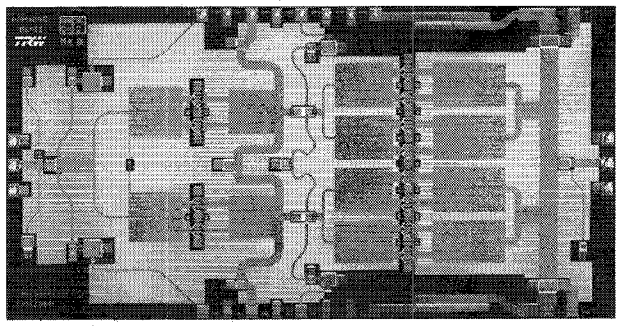

Fig. 1. 1-W Q-band MMIC power amplifier.

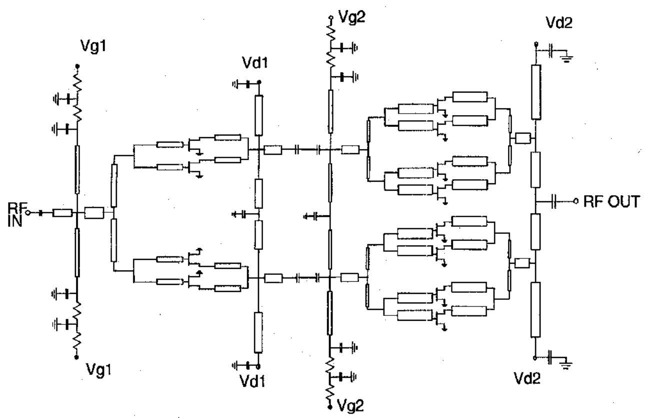

Fig. 2. Schematic diagram of MMIC power amplifier.

Manuscript received August 8, 1994.
The authors are with TRW Electronics Systems and Technology Division, Redondo Beach, CA 90278 USA.
IEEE Log Number 9407041.

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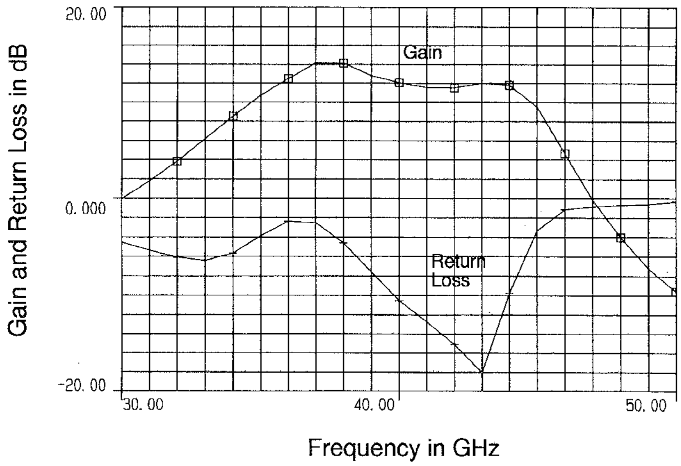

Fig. 3. Measured small signal gain and return loss versus frequency.

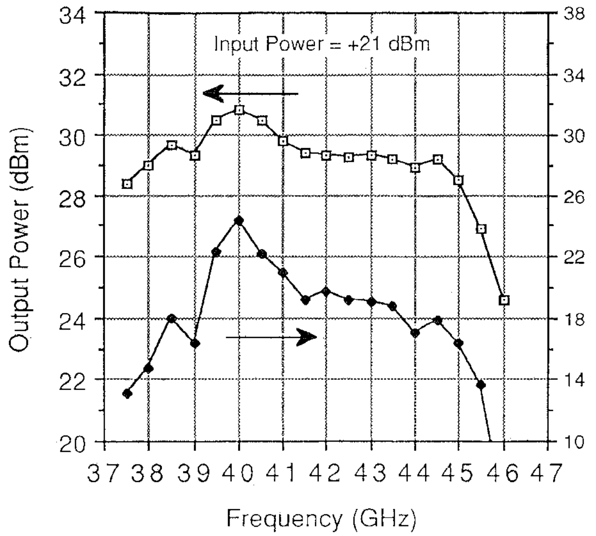

Fig. 4. Measured output power and efficiency versus frequency.

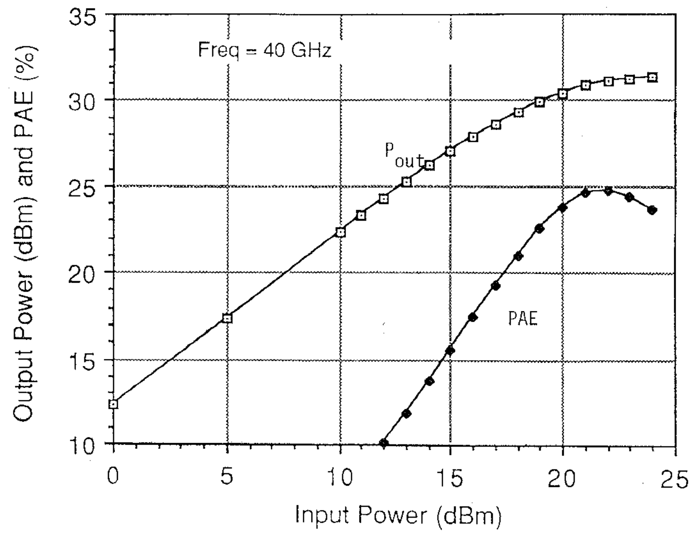

Fig. 5. Measured compression data versus input power.

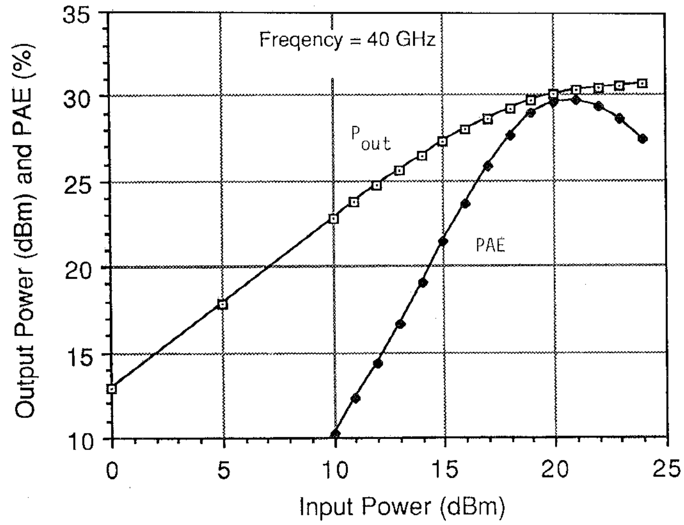

Fig. 6. Measured output power and efficiency versus input power when drain voltage is at 4 V.

III. Measured Result

On-wafer probe screening measurement was first conducted to examine the linear performance of the power amplifier. In this case, the drain stages were biased at class AB condition with a drain voltage at 3 V. Fig. 3 shows the measured small-signal gain and the input return loss versus frequency. The linear gain is above 12 db from 38–44 GHz and has a peak of 15 dB at 38 GHz.

The power measurement was done by using a waveguide setup. Finline transitions were used to bridge the MMIC chip and waveguide measurement system and the back-to back fixture loss was measured to be 0.6 dB at Q band. Fig. 4 presents the measured output power and power-added-efficiency as a function of frequency. The output power is peaked at 40 GHz and measured to be 1.2 W with 25% efficiency. From 39–41 GHz, the measured output power is higher than 1 W with a associated gain higher than 9 dB. Fig. 5 shows the measured compression data as a function of input power at 40 GHz. The peak efficiency (25%) occurs when the input power is 21 dBm. In the above case, the drain voltage is biased at 5 V and the gate is biased at 75% Gm peak condition. If the drain voltage is reduced to 4 V, the power added efficiency is increased to 29.4% with 1 W output power at 40 GHz. The measured output power and efficiency versus the input power when $V_D = 4$ V is presented in Fig. 6.

IV. Conclusion

The MMIC HEMT power amplifier presented in this paper delivers over 1 W with the highest efficiency at this power level ever reported in Q-band power amplifier design. The state-of-the-art power amplifier chip is achieved by combining highly efficient InGaAs PHEMT's with optimum matching circuit topology. Many Q-band applications, such as terminal and transmitted phased array, can be benefited from this work.

Acknowledgment

The authors wish to thank R. Lai for his effort on processing MMIC amplifier and D. Garske for her work on measurement. Also, the advice received from B. Allen and M. Aust was valuable during the design phase. Finally, this work was developed on TRW internal IR&D funds.

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